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FACSIMILE COVER SHEET

X	FACSIMILE COVER SHEET	___	AMENDMENT (# Pages)
___	NEW APPLICATION	X	EOT (# Month)
___	DECLARATION (# Pages)	___	NOTICE OF APPEAL
___	ASSIGNMENT (# Pages)	X	APPEAL (11 Pages)
___	FORMAL DRAWINGS	___	ISSUE FEE (# Pages)
___	INFORMAL DRAWINGS	___	CHANGE IN CORRESPONENCE ADDRESS
___	CONTINUATION APP'N (# Pages)		
___	DIVISIONAL APP'N		

NAME OF INVENTOR(S):
Ano

RECEIPT DATE & SERIAL NO.:
Serial No.: 10/017,737
Filing Date: 12/14/2001

TITLE OF INVENTION:
STACKED IC PACKAGE

TI FILE NO.:	DEPOSIT ACCT. NO.:
TI-33183	20-0668

FAXED: 1-17-06
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Ano	Docket No:	TI-33183
Serial No:	10/017,737	Examiner:	Lewis, Monica
Filed:	12/14/2001	Art Unit:	2822
For:	STACKED IC PACKAGE		

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APPEAL BRIEF PURSUANT TO 1.192(c)

CERTIFICATION OF FACSIMILE TRANSMISSION

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Tommie Chambers

Tommie Chambers

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

The following Appeal Brief is respectfully submitted in connection with the above identified application in response to the final rejection mailed May 18, 2005, and the Advisory Action mailed October 3, 2005.

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated.

RELATED APPEALS AND INTERFERENCES

Appellants legal representative knows of no appeals or interferences which will be directly affected, or have a bearing on the Board's decision.

STATUS OF THE CLAIMS

Claims 1-30 were originally filed with Claims 6, 11-20, 22, and 27 being subsequently cancelled.

Consequently the subject matter of the instant appeal is the final rejection of Claims 1-5, 7-10, 21, 23-26, and 28-30.

STATUS OF AMENDMENTS

The application was originally filed with Claims 1-30.

A response after final rejection was filed on September 16, 2005, amending no claims.

The Advisory Action did not indicate that the response had been entered but appears to respond to it.

SUMMARY OF THE CLAIMED SUBJECT MATTER

Referring now to Figure 2 there is illustrated a multiple stacked IC chip arrangement in accordance with an exemplary embodiment of the present invention. In this embodiment, the chip module includes at least a lower chip 10 having a bottom and top surface and a upper chip 30 having a bottom and top surface. The bottom of the upper chip 30 is stacked atop the top of the lower chip 10 in which the bottom of the lower chip 10 is connectable to a circuit board 40 or other substrate. Note that the upper chip 30 is stacked directly on top of the lower chip 10 (such that there is no overhang) and that the chips are approximately the same size. Figure 4 shows the top view of the stacked arrangement illustrated in Figure 2. Note that the bonding pads of

the lower chip 10 are completely covered by the upper chip 30 and that the lower chip 10 does not extend out beyond the perimeter of the upper chip 30.

The chips (10 and 30) have bonding pads located on the outside perimeter of each respective top surface. Electrical connection of the stacked chip module to the circuit board 40 can be performed by wire bonding or other similar techniques. The two chips are advantageously attached together via a die attach material 220 applied on the bottom surface of the upper chip 30 prior to applying the upper chip 30 to the stack. A layer of the die attach material 220 is applied across the entire upper chip bottom surface such that when the upper chip 30 is place on the stack the bonding pads of the lower chip 10 are completely covered.

The die attach material 220 is a thermosetting material which become soft when heated and rigid when subsequently cooled. Further, in at least one embodiment, the thermosetting material is a semi conducting material. Prior to pressing the upper chip 30 onto the lower chip 10, the die attach material 220 is heated to become pliable. Subsequently, the upper chip 30 is pressed onto the lower chip 10 and the die attach material 220 conforms around the bonding pads of the lower chip 10. When cooled, the die attach material 220 becomes rigid and attachment is complete. This process can be repeated for each of a plurality of chips. The thickness of the die attach material 220 is selected such that there is electrical disconnection from the upper chip 30 and the wire bond of the lower chip 10 when the upper chip 30 is pressed to its final position. For example, with a semi conducting material, there should be at least a 10 μm gap between the wire bond of the lower chip 10 and the upper chip 30 to provide electrical disconnection. The chip module can obviously include more that two chips by repeating the above-described process for each successive chip.

The die attach thickness can vary depending on the bonding method used on the lower chip 10. For example, where ball bonding is first applied to the chip (as shown in Figure 1) the wire loop is greater than if the bonding is reversed and the ball bonding is first applied to the circuit board or substrate. For wire bonding of the type shown in Figure 1, the die attach thickness is approximately 150 μm to approximately 200 μm.

For the wire bonding of the type shown in Figures 2, the die attach thickness is approximately 70 μm to approximately 100 μm.

The present approach not only advantageously protects the wire bond of the lower chip 10 during attachment, but also encapsulates the wire bond to protect from future possible physical damage. This approach can also reduce the production distance between stacked chips and the overall height of the chip module.

Referring now to Figure 3 there is illustrated a multiple stacked IC chip arrangement in accordance with another exemplary embodiment of the present invention. In this embodiment, the chip module includes at least a lower chip 10 having a bottom and top surface and a upper chip 30 having a bottom and top surface. The bottom of the upper chip 30 is stacked atop the top of the lower chip 10 in which the bottom of the lower chip 10 is connectable to a circuit board 40 or other substrate. Note that the upper chip 30 is stacked directly on top of the lower chip 10 (such that there is no overhang) and that the chips are approximately the same size, as shown in Figure 4.

The difference between this embodiment and that shown in Figure 2 is the addition of a layer of an insulation material 230 applied to the bottom surface of the upper chip 30 prior to the application of the die attach material 220. The insulation material 230 is applied across the entire upper chip bottom surface. Similar to that described above, a layer of the thermosetting die attach material 220 is then applied across the entire upper chip bottom surface area such that when the upper chip 30 is place on the stack the bonding pads of the lower chip 10 are completely covered.

Prior to pressing the upper chip 30 onto the lower chip 10, the die attach material 220 is heated to become pliable. Subsequently, the upper chip 30 is pressed onto the lower chip 10 and the die attach material 220 conforms around the bonding pads of the lower chip 10. After a period of time for cooling, the die attach material 220 becomes rigid. The thickness of the insulation material layer and the die attach material is cooperatively selected such that there is electrical disconnection from the upper chip 30 and the wire bond on the lower chip 10 when the upper chip 30 is pressed to its final position and the final distance between the stacked chips is minimalized.

In one embodiment, the insulation material 230 is an inorganic material, such as SiO2 (silicon dioxide), with a thickness of approximately 1 μm. In another embodiment, the insulation material 230 is an organic material, such as epoxy, with a thickness of approximately 5 μm to approximately 100 μm. Regardless of the thickness of the insulation layer 230, the thickness of the die attach layer 220 is preferably approximately 70 μm to 200 μm depending on the type of bonding used on the lower chip 10. The thickness of the die attach layer 220 is less in the embodiment illustrated in Figure 3 because an electrical disconnection gap is provided by the insulation layer.

GROUNDS OF REJECTION

The two issues on appeal are first whether Claims 1, 3-5, 7, 8, 10, 21, 23-26, and 28-30 are anticipated under 35 U.S.C. § 102(a) by Derderian; and secondly whether Claims 2 and 9 are unpatentable over Derderian.

These rejections are traversed.

ARGUMENTS

It is respectfully submitted that Derderian does not disclose or suggest the presently claimed invention including a first attached layer to directly couple the first chip and the second chip in the various forms in independent Claims 1 and 21.

The Honorable Board's attention is directed to Figure 9 of Derderian where spacers 22 between the layers are shown.

The spacers result in a higher profile combination.

In contrast the present invention has a low profile.

It is respectfully submitted that Claims 1-5, 7-10, 21, 23-26, 28-30 are allowable over the applied art.

CONCLUSION

For the foregoing reasons, Appellant respectfully submits that the Examiner's final rejection of Claims 1-5, 7-10, 21, 23-26, and 28-30 under 35 U.S.C. § 102 and 35 U.S.C. § 103 is not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,

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APPENDIX

Claim 1 (previously presented): A multichip module comprising:

a first chip having opposing top and bottom surfaces and having bonding pads located on a perimeter of said top surface, each of said bonding pads operable for bonding a wire;

a second chip having opposing top and bottom surfaces and having bonding pads located on a perimeter of said top surface, each of said bonding pads operable for bonding a wire;

a first attach layer having an area equal to an area of said second chip bottom surface for directly coupling said first chip and said second chip, said first attach layer covering said each of said bonding pads on said first chip and having a thickness to provide electrical disconnection of said first chip wire bonds and said second chip, said first attach layer is applied to said second chip bottom surface prior to coupling said first chip and said second chip; and

a second attach layer having an area equal to said second chip bottom surface area and disposed between said first attach layer and said second chip bottom surface, said second attach layer being an insulating material having a thickness and cooperable with said first attach layer to provide electrical disconnection of said first chip wire bonds and said second chip.

Claim 2 (original): The multichip module of Claim 1, wherein said electrical disconnection is provided as a gap between said first chip wire bonds and said second chip, and wherein said gap is approximately 10 μm.

Claim 3 (original): The multichip module of Claim 1, wherein said first attach layer is a thermosetting material, wherein said thermosetting material is pliable for coupling said first chip and said second chip such that said thermosetting material conforms to said first chip wire bond.

Claim 4 (original): The multichip module of Claim 1, wherein said first chip top and bottom surfaces and said second chip top and bottom surfaces have equal areas.

Claim 5 (original): The multichip module of Claim 1, wherein said first chip and said second chip have a stacked arrangement such that said first chip bonding pads are covered from above by said second chip.

Claim 6 (cancelled)

Claim 7 (previously presented): The multichip module of Claim 1, wherein said first attach layer is a thermosetting material, wherein said thermosetting material is pliable for coupling said first chip and said second chip such that said thermosetting material conforms to said first chip wire bond and said second attach layer is silicon dioxide.

Claim 8 (previously presented): The multichip module of Claim 1, wherein said electrical disconnection is provided as a gap between said first chip wire bonds and said second chip, and wherein said gap is approximately equal to said second attach layer thickness.

Claim 9 (previously presented): The multichip module of Claim 1, wherein said second attach layer thickness is approximately 1 μm.

Claim 10 (previously presented): The multichip module of Claim 6, wherein said first chip top and bottom surfaces and said second chip top and bottom surfaces have equal areas, and wherein said first and second chips are stacked such that said first chip bonding pads are covered from above by said second chip.

Claims 11-20 (cancelled)

Claim 21 (previously presented): A multichip module, comprising:

a first chip having opposing top and bottom surfaces and having first bonding pads located on a perimeter of said top surface;

a wire having a bond to one of said first bonding pads;

a second chip having opposing top and bottom surfaces and positioned with said bottom surface of said second chip adjacent said top surface of said first chip;

a first attach layer to directly couple said top surface of said first chip and said bottom surface of said second chip and covering said wire bond, said first attach layer having an area substantially equal to the area of said second chip; and

a second attach layer adjacent to said bottom surface of said second chip and between said bottom surface of said second chip and said first attach layer.

Claim 22 (cancelled)

Claim 23 (previously added): The multichip module of Claim 21, wherein said first attach layer is a thermosetting material.

Claim 24 (previously added): The multichip module of Claim 21, wherein said second attach layer is an inorganic material.

Claim 25 (previously added): The multichip module of Claim 21, wherein said first and second chips are approximately the same size.

Claim 26 (previously added): A multichip module, comprising:

a substrate having a plurality of contact pads;

a first chip having opposing top and bottom surfaces and having first bonding pads located on a perimeter of said top surface, said first chip mounted on said substrate;

a wire having a ball bond to one of said plurality of contact pads on said substrate and a bond to one of said first bonding pads;

a second chip having opposing top and bottom surfaces and positioned with said bottom surface of said second chip adjacent said top surface of said first chip;

a first attach layer between said top surface of said first chip and said bottom surface of said second chip and covering said wire bond to said one of said first bonding pads, said first attach layer having an area substantially equal to the area of said second chip;

a second attach layer adjacent to said bottom surface of said second chip and between said bottom surface of said second chip and said first attach layer.

Claim 27 (cancelled)

Claim 28 (previously added): The multichip module of Claim 26, wherein said first attach layer is a thermosetting material.

Claim 29 (previously added): The multichip module of Claim 26, wherein said second attach layer is an inorganic material.

Claim 30 (previously added): The multichip module of Claim 26, wherein said first and second chips are approximately the same size.

EVIDENCE APPENDIX

Appellants are submitting no items of evidence.

RELATED PROCEEDINGS APPENDIX

Appellants have no submission for the Related Proceeding Appendix.